IN THE CLAIMS:

Please amend the claims as follows:

1-16. (Canceled)

17. (Currently Amended) A signal transmission system comprising:

a write amplifier;

a sense amplifier connected to the write amplifier via a data bus; and

a semiconductor memory device for writing data from the write amplifier to the sense amplifier, the semiconductor memory comprising a signal transmission line for transmitting data without requiring precharging for every bit, wherein when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein said signal transmission line comprises a plurality of switchable signal transmission lines organized in a branching structure or a hierarchical structure, at least one target unit from which to read data is connected to each of said plurality of switchable signal transmission lines;

a readout circuit for eliminating an intersymbol interference component is connected to said signal transmission line; and

an intersymbol interference component elimination circuit for reducing noise introduced when said signal transmission line is switched between said plurality of switchable signal transmission lines, and thereby provides a smooth intersymbol

interference component elimination operation when said signal transmission line is switched,

wherein said at least one target unit is [[a]] said sense amplifier for reading data out of a memory cell, and said readout circuit is a data bus amplifier having an intersymbol interference component elimination function.

18. (Currently Amended) A signal transmission system as claimed in claim 17, wherein said data bus amplifier and said sense amplifier are connected via a column gate which is controlled by said select signal.

19. (Currently Amended) A signal transmission system as claimed in claim 17, wherein during said writing, after transferring data to said sense amplifier for writing therein, said bit line disconnected from said sense amplifier is reconnected to said sense amplifier, the data written in said sense amplifier is transferred for writing into [[a]] said memory cell selected by a memory cell selection line from among memory cells connected to said bit line, and thereafter said memory cell selection line is deselected, thereby storing data in said memory cell.

20. (Currently Amended) A semiconductor memory device employing a signal transmission system for transmitting data comprising:

a signal transmission line for transmitting data without requiring precharging for every bit, wherein said signal transmission line comprises a plurality of switchable signal transmission lines organized in a branching structure or a hierarchical structure, at least one target unit from which to read data is connected to each of said plurality of switchable signal transmission lines;

a readout circuit including a circuit for eliminating an intersymbol interference component is connected to said signal transmission line; and

an intersymbol interference component elimination circuit for reducing noise introduced when said signal transmission line is switched between said plurality of switchable signal transmission lines, and thereby provides a smooth intersymbol interference component elimination operation when said signal transmission line is switched,

wherein said at least one target unit is a sense amplifier for reading data out of a memory cell, and said readout circuit is a data bus amplifier having an intersymbol interference component elimination function.

21. (Original) A semiconductor memory device as claimed in claim 20, wherein the response time of said signal transmission line is set approximately equal to or longer than the length of a transmitted symbol.

22. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein, when transferring continuous data from the same signal transmission line, precharging of said signal transmission line for every bit is not performed, and during a period preceding the switching of said signal transmission line and during a period when continuous data transmission is not performed, some of said plurality of switchable signal transmission lines are precharged to a predetermined voltage level.

23. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein, when switching from a first signal transmission line to a second signal transmission line, said second signal transmission line to be selected next is

precharged to a predetermined voltage level before switching to said second signal transmission line.

24. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein said readout circuit employs a partial-response detection method, and said readout circuit employing said partial-response detection method corrects the intersymbol interference component elimination function when said signal transmission line is switched, by varying an input capacitance value.

25. (Original) A semiconductor memory device as claimed in claim 24, wherein said readout circuit employing said partial-response detection method includes: an intersymbol interference estimation means for estimating intersymbol interference from a previously received signal; and a decision means for making a logic decision on a currently received signal by subtracting said estimated intersymbol interference from said currently received signal.

26. (Previously Presented) A semiconductor memory device as claimed in claim 24, wherein said readout circuit employing said partial-response detection method includes first and second partial-response detection amplifiers arranged in parallel with each other, and wherein said first partial-response amplifier performs an intersymbol interference estimation operation while said second partial-response detection amplifier is performing a data decision operation and, at the next timing, said first partial response amplifier performs the data decision operation while said second partial-response detection amplifier is performing the intersymbol interference estimation operation.

27. (Currently Amended) A semiconductor memory device as claimed in claim 20, wherein said signal transmission line is configured as complementary buses and said readout circuit is configured as a complementary-type data bus amplifier.

28. (Original) A semiconductor memory device as claimed in claim 20, wherein said readout circuit operates only when data is transferred via said signal transmission line.

29. (Original) A semiconductor memory device as claimed in claim 20, wherein, when switching said signal transmission line, a first driver select signal for selecting a driver on an activated signal transmission line currently transmitting data thereon and a second driver select signal for selecting a driver on a signal transmission line currently inactive and expected to be activated after the switching are generated as a common driver select signal, and said inactive signal transmission line is precharged during a period that includes the last cycle of the state in which data in an arbitrary driver on said inactive signal transmission line, selected simultaneously when selecting a driver on said activated signal transmission line, is transmitted on said inactive signal transmission line.

30. (Previously Presented) A semiconductor memory device as claimed in claim 29, wherein said common driver select signal is also supplied in common to said plurality of switchable signal transmission lines other than said signal transmission line expected to be activated next.

31. (Original) A semiconductor memory device as claimed in claim 20, wherein a timing signal for carrying out the switching of said signal transmission line is generated externally and distributed to a switching circuit for each signal transmission

line, or is supplied at a timing before the last one cycle of amplification of a currently activated signal transmission line.

32. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein before switching said signal transmission line, an inactive signal transmission line is precharged in such a direction as to reduce the noise that has an effect on an intersymbol interference component elimination operation subsequently performed in said readout circuit, or precharged to a voltage level within a range of plus or minus a predetermined voltage about a voltage at one half of either a read or write maximum amplitude of said signal transmission line, said predetermined voltage being smaller than a transistor threshold voltage.

33. (Currently Amended) A semiconductor memory device as claimed in claim 20, wherein said signal transmission system includes a state latch circuit for holding at least two states consisting of a CURRENT state indicating a bus currently in an active state and a NEXT state indicating [[a]] the bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating [[a]] the bus in a standby state, and a PREVIOUS state indicating [[a]] the bus just deactivated.

34. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein said sense amplifier for reading data out of said memory cell also functions by itself as a drive circuit for a data bus.

35. (Original) A semiconductor memory device as claimed in claim 20, wherein said semiconductor memory device is a dynamic random-access memory.

36. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein from said sense amplifier the data is first transferred onto a local data bus via a selected column gate, and then onto a global data bus via a local data bus switch that selects said local data bus, and said data is amplified by a complementary-type data bus amplifier having the intersymbol interference component elimination function, thereby continuing data transmission uninterruptedly without performing data bus precharge during data transfer.

37. (Currently Amended) A semiconductor memory device as claimed in claim 20, wherein a read-select pulse width of a read select signal for selecting the connection between said at least one target unit and a data bus for data read is made shorter than a write-select pulse width of a write select signal for selecting the connection between said at least one target unit and said data bus for data write.

38. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein during a continuous cycle period, whether read or write cycles, data bus precharge is rendered unnecessary at least for activated buses.

39. (Previously Presented) A semiconductor memory device as claimed in claim 20, wherein in any data bus state except for [[a]] continuous read and write cycle periods, a read precharge level is set at a different level than a write precharge level.

40. (Previously Presented) A semiconductor memory device employing a signal transmission system for transmitting data without requiring precharging comprising:

a signal transmission line for transmitting data without requiring precharging for every bit, said signal transmission line comprises a plurality of switchable transmission

lines, and when said signal transmission line is switched from a first transmission line to a second transmission line, said second transmission line to be selected next is precharged to a predetermined level before switching to said second transmission line, in order to continue data transmission;

a target unit that is a sense amplifier for reading data out of a memory cell; and

a readout circuit that is a data bus amplifier having an intersymbol interference component elimination function.

41. (Currently Amended) A semiconductor memory device as claimed in claim 40, further comprising a state latch circuit for holding at least two states consisting of a CURRENT state indicating a bus currently in an active state and a NEXT state indicating [[a]] the bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating the bus in a standby state, and a PREVIOUS state indicating the bus just deactivated.

42. (Currently Amended) A semiconductor memory device as claimed in claim 40, wherein said sense amplifier for reading data out of said memory cell also functions by itself as a drive circuit for [[said]] a data bus.

43. (Original) A semiconductor memory device as claimed in claim 40, wherein said semiconductor memory device is a dynamic random-access memory.

44. (Previously Presented) A semiconductor memory device as claimed in claim 40, wherein from said sense amplifier, the data is first transferred onto a local data bus via a selected column gate, and then onto a global data bus via a local data bus switch that selects said local data bus, and said data is amplified by a complementary-type data bus amplifier having the intersymbol interference component elimination

function, thereby continuing data transmission uninterruptedly without performing data bus precharge during data transfer.

45. (Currently Amended) A semiconductor memory device as claimed in claim 40, wherein a read-select pulse width of a read select signal for selecting a connection between said target unit and [[said]] a data bus for data read is made shorter than a write-select pulse width of a write select signal for selecting the connection between said target unit and said data bus for data write.

46. (Previously Presented) A semiconductor memory device as claimed in claim 40, wherein during a continuous cycle period, whether read or write cycles, data bus precharge is rendered unnecessary at least for activated buses.

47. (Previously Presented) A semiconductor memory device as claimed in claim 40, wherein in any data bus state except for continuous read and write cycle periods, a read precharge level is set at a different level than a write precharge level.

48. (Canceled)

49. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating [[the]] a bus in a standby state, and a PREVIOUS state indicating [[the]] a bus just deactivated,

wherein each of said blocks cycles through the four states, changing state from the STANDBY state to the NEXT state to the CURRENT state to the PREVIOUS state and then back to the STANDBY state.

50. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating [[the]] a bus in a standby state, and a PREVIOUS state indicating [[the]] a bus just deactivated,

wherein when [[one]] a block of said plurality of blocks is in the STANDBY state, a signal input for raising a word line within said block is enabled; when said block is in the NEXT state, said block is in a state ready to read data from a unit target or a sense amplifier onto a bus or ready to write data to the unit target or the sense amplifier, with said word line rising and said sense amplifier activated at least at the end of said NEXT state ~~period~~; when said block is in the CURRENT state, data is being read out of or being written in said block; and when said block is in the PREVIOUS state, data is rewritten, and then said word line is lowered and a bit line is precharged.

51. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state,

said_NEXT state, a STANDBY state indicating [[the]] a bus in a standby state, and a PREVIOUS state indicating [[the]] a bus just deactivated,

wherein, when performing a data write operation, a switch connecting a sense amplifier to a bit line is turned off near the end of the period when [[one]] a block of said plurality of blocks is in the NEXT state and, while maintaining an off state during the CURRENT state, a data write sense amplifier connected to a data bus writes data into the sense amplifier connected to a memory cell where the data is to be written; when a transition is made from the CURRENT state to the PREVIOUS state, said switch connecting said sense amplifier to said bit line is turned on and, during a portion of the period of the PREVIOUS state, the data held in said sense amplifier is written into said memory cell via said bit line, after which a word line is lowered, said sense amplifier is deactivated, and said bit line is precharged, said block then entering the STANDBY state.

52. (Original) A semiconductor memory device as claimed in claim 51, wherein an external access is not allowed to memory cell arrays of said block during the period when said block is in said PREVIOUS state.

53. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating [[the]] a bus in a standby state, and a PREVIOUS state indicating [[the]] a bus just deactivated,

wherein said state latch circuit is provided for each of said plurality of blocks .

54. (Currently Amended) A semiconductor memory device comprising:

a plurality of blocks; and

a state latch circuit for holding at least two states consisting of a CURRENT state indicating [[the]] a bus currently in an active state and a NEXT state indicating [[the]] a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating [[the]] a bus in a standby state, and a PREVIOUS state indicating [[the]] a bus just deactivated,

further including an operation signal generating circuit for generating a plurality of operation signals for use within each of said plurality of blocks from state signals output from said state latch circuit for each of said plurality of blocks.

55. (Previously Presented) A semiconductor memory device as claimed in claim 54, wherein said operation signal generating circuit generates a row address latch signal by using a state signal indicating the NEXT state out of the state signals output from said state latch circuit for each of said plurality of blocks.

56. (Previously Presented) A semiconductor memory device comprising:

a plurality of row blocks, wherein each of said plurality of row blocks has a local data bus; and

a selection switch for selectively controlling the local data bus, and for connection to a global data bus at a hierarchically upper level,

wherein a period is provided during which at least two of said plurality of row blocks are active at the same time and, when said local data bus is switched between

the row blocks that are activated at the same time during said period, data on said global data bus transferred from said local data bus are continuously read out.

57. (Currently Amended) A semiconductor memory device as claimed in claim 56, further comprising:

a memory cell [[or]] and a sense amplifier for reading data in said memory cell transfers data onto said local data bus by a row selection line and a column select signal, wherein the local data bus is selected in accordance with a row block select signal, and at least one local data bus is connected to said global data bus; and

a complementary-type partial response detection bus amplifier connected to said global data bus, wherein an intersymbol interference component on said global data bus is eliminated, thereby providing high-speed data read.

58. (Currently Amended) A semiconductor memory device as claimed in claim 56, including a holding circuit which, after switching is made from a first local data bus to a second local data bus, holds [[the]] a selected state of the row selection line in the row block having said first local data bus for a prescribed amount of time, thus enabling the local data bus switching between a plurality of activated row blocks.

59. (Currently Amended) A semiconductor memory device as claimed in claim 58, further including a decoder and a row selection line holding circuit which latches a row address into said decoder in accordance with a row address latch signal given to each row block, selects a designated row selection line within said each row block, and holds said row selection line in its selected state for a prescribed amount of time or until a signal for initializing said decoder is input.

60. (Previously Presented) A semiconductor memory device as claimed in claim 59, wherein said decoder and said row selection line holding circuit share address lines with other decoders and other row selection line holding circuits provided for other row blocks, latch said address signal and select the designated row selection line in the block for which the row address latch signal given to each of said row blocks is valid, and prevent row selection lines from transitioning in other blocks for which said row address latch signal is not valid.

61. (Currently Amended) A semiconductor memory device as claimed in claim 59, wherein said decoder and said row selection line holding circuit comprise a dynamic logic circuit and a switch means for controlling the activation of said dynamic logic circuit, and when said row address is input at an input of said dynamic logic circuit, and said switch means is on, transition of a data decoder output section is enabled, and when said switch means is off, transition of said data decoder output section is prohibited to hold the state of said row selection line.

62. (Previously Presented) A semiconductor memory device as claimed in claim 61, wherein said decoder and said row selection line holding circuit hold the state of said row selection line for a finite amount of time.

63. (Previously Presented) A semiconductor memory device as claimed in claim 59, wherein said decoder and said row selection line holding circuit include the holding circuit, provided for each row block, for holding the address to be input to said decoder for each row block, and hold the state of said row selection line by holding said address for each row block.

64. (Currently Amended) A semiconductor memory device as claimed in claim 58, wherein said row selection line is a word line in [[an]] a memory cell array.

65. (Canceled)

66. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein said bit line disconnection is performed in such a manner that, during a period when write cycles are performed continuously with a plurality of sense amplifiers within a same block being selected sequentially, said plurality of sense amplifiers remain disconnected from their associated bit lines, and when the continuous write within the same block is completed, said disconnected bit lines are reconnected to their associated sense amplifiers.

67. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein during said writing, after transferring data to said sense amplifier for writing therein, said bit line disconnected from said sense amplifier is reconnected to said sense amplifier, the data written in said sense amplifier is transferred for writing into a memory cell selected by a memory cell selection line from among memory cells connected to said bit line, and thereafter said memory cell selection line is deselected, thereby storing data in said memory cell.

68. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein said sense amplifier is configured as a CMOS complementary type, and two N-channel MOS transistors are used as a column selection gate connected to complementary buses, and wherein the ratio of P-channel MOS transistors of said

sense amplifier to the N-channel MOS transistors of said column selection gate is made small so that data on a low voltage side of said complementary buses is written.

69. (Canceled)

70. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein, when switching from a row block to another, local data buses in the row block where writing is completed are precharged to prevent an erroneous write in a write-completed block.

71. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier,

thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein at least during writing to said sense amplifier, a maximum value of data on a high voltage side of said data bus is set lower than a source voltage of a P-channel MOS transistor of said sense amplifier in an activated state or a maximum voltage of said data bus in a read state, and higher than one half of said maximum voltage.

72. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein a maximum value of the data on a high voltage side of said data bus that a final-stage driver in said write amplifier outputs is clamped at a predetermined voltage near said sense amplifier regardless of an output level of said write amplifier.

73. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein after activating a selected row block, said data bus is precharged before writing data to a first sense amplifier and after writing data is done to a final sense amplifier.

74. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein the data bus precharges before supplying said select signal is rendered unnecessary at least during a period when a plurality of continuous write cycles are being performed.

75. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

said semiconductor device further includes a latch-type sense amplifier, and the connection between said sense amplifier and said bit line is controlled by a bit line transfer gate with a control signal applied to said bit line transfer gate and operated quickly for disconnection and slowly for connection.

76. (Original) A semiconductor memory device as claimed in claim 75, wherein the control signal applied to said bit line transfer gate is formed so that said bit line rises slowly or in a steplike manner in order to prevent inversion of data latched in said sense amplifier.

77. (Previously Presented) A semiconductor memory device as claimed in claim 76, wherein the control signal applied to said bit line transfer gate is generated by being delayed through delay means so that said control signal rises slowly, or is generated by a circuit having a plurality of switching transistors whose sources are coupled to different voltages or whose gates are supplied with different control voltages so that said control signal rises in the steplike manner.

78. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein a read-select pulse width of a read select signal for selecting a connection between a target unit and said data bus for data read is made shorter than a write-select pulse width of a write select signal for selecting the connection between said target unit and said data bus for data write.

79. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein during a continuous cycle period, whether read or write cycles, data bus precharge is rendered unnecessary at least for activated buses.

80. (Previously Presented) A semiconductor memory device comprising:

a write amplifier; and

a sense amplifier coupled to the write amplifier via a data bus, wherein data is written from the write amplifier to the sense amplifier, and

when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier,

wherein in any data bus state except for plurality of continuous read and write cycle periods, a read precharge level is set at a different level than a write precharge level.

81-100. (Canceled).